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Reg. No. : .....

Name : .....

Fifth Semester B.Tech. Degree Examination, November 2012
(2008 Scheme)
08.503 : COMPUTER ORGANISATION AND ARCHITECTURE (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions in Part – **A**, **each** question carries **4** marks.

1. Distinguish between Harvard architecture and Von-Neumann architecture.
2. Explain pseudo direct addressing mode with an example.
3. A program runs in 20 seconds on computer 'A' which has a 8 GHz clock. Another computer 'B' is built that will run this program in 12 seconds. For this, computer B requires 2-4 times as many as clock cycles as computer A for this program. What is the clock rate of B ?
4. Draw the data path for branch instruction in MIPS implementation.
5. Explain how multiple levels of control is implemented in MIPS architecture . What are its advantages ?
6. What are structural hazards ? Illustrate with an example.
7. Discuss DMA data transfer scheme.
8. Distinguish between write through and write back protocol.
9. Write the functions of the following pins of 8086.
   1) $\overline{\text{TEST}}$ 2) $\overline{\text{RQ}}$ / $\overline{\text{GTO}}$
   3) $\overline{\text{LOCK}}$ 4) $\overline{\text{DEN}}$
10. Explain memory interleaving. What is its significance ?

P.T.O.

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. Multiply 0101101 by 0011110 using Booth algorithm.

12. Showing all the steps add the numbers 0.5_{10} and -0.4375_{10} in binary.

13. a) Divide 1000 by 0011 using restoring and non restoring division algorithm.

    b) Draw the hardware implementation of restoring and non restoring division algorithm.

Module – II

14. a) Differentiate between single cycle and multicycle implementation.

    b) Explain edge triggered clocking methodology.

15. With the help of diagram and necessary control signals, explain multi cycle implementation scheme.

16. a) Explain how super scalar execution increase instruction through put, in a computer. 4

    b) Explain pipelined datapath. 6

Module – III

17. With suitable examples, explain the different addressing modes of 8086.

18. With necessary illustrations, explain different memory mapping techniques.

19. What is virtual memory ? Discuss in detail, about how address translation is carried out in virtual memories.